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<u>L24</u>	L22 and l6	63	<u>L24</u>
<u>L23</u>	L22 and l5	7	<u>L23</u>
<u>L22</u>	l19 and (extend\$3 or extension\$1 or delay\$3 or wait) near5 (cycle\$1 or period\$1 or clock\$3 or slot\$1)	241	<u>L22</u>
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<u>L21</u>	(712/36)[CCLS]	260	<u>L21</u>
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L19 12 and (ASIC or application near1 specific)

512 L19

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L18 13 and 19

3 L18

L17 13 and 18

0 L17

L16 13 and 17

9 L16

L15 13 and 16

125 L15

L14 13 and 15

63 L14

L13 15 and 19

0 L13

L12 15 and 18

0 L12

L11 15 and 17

3 L11

L10 15 and 16

31 L10

L9 (710/266 ) [CCLS]

237 L9

L8 (713/401 ) [CCLS]

454 L8

L7 (712/227,248) [CCLS]

731 L7

L6 (712/2-300) [CCLS]

11162 L6

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L5 L3 and (extend\$3 or extension\$1 or delay\$3 or wait) near5 (cycle\$1 or period\$1 or clock\$3 or slot\$1)

63 L5

L4 L3 near35 (extend\$3 or extension\$1 or delay\$3 or wait) near5 (cycle\$1 or period\$1 or clock\$3 or slot\$1)

2 L4

L3 L2 near15 return\$5

247 L3

L2 interrupt\$5 near8 exception\$1

3552 L2

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L1 6167479.pn.

1 L1

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Smith, J.E.; Pleszkun, A.R.;  
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**26. Design and Implementation of a series voltage sag compensator under practical utility conditions**

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